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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,527	05/23/2001	Kenneth Mark Wilson	HP-10012389	3037

7590 06/03/2003
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

NGUYEN, THAN VINH

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 06/03/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/864,527	WILSON ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____. | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-23 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3,5-17,19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Kleinsorge et al (US 6,247,109) .

As to claim 1,14:

Kleinsorge teaches a system having a partitioned memory, said system comprising:

a processor (CPU; Figure 4);

a hardware implemented memory router coupled to said processor; memory coupled to said memory router (memory map); said memory router configured to store memory partition

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information, said information describing the memory allocated to said processor; and said memory router operable to map a memory access request having an address from said processor to an address in said memory allocated to said processor (system manager performs memory map of partitions assigned to CPUs; Abs; 4/60-66).

As to claim 2:

Kleinsorge teaches at least a second processor coupled to said memory router, wherein said system comprises a plurality of processors (plural CPUs); said memory partition information stored in said memory router further describes the memory allocated to each of said plurality of processors; and said memory router is further operable to map memory access requests from said plurality of processors to respective addresses in said memory allocated to each of said plurality of processors (assigning partitions to plural CPUs; 4/55-65).

As to claim 3,22:

Kleinsorge teaches said memory partition information further describes the type of access each processor of said plurality has to each portion of its allocated memory; and said memory router is further operable to determine whether a memory access request having a first address from a first processor of said plurality is valid for said first address, based on the type of access and said first address (access type restriction; 12/55-62).

As to claims 5,6,15,17,19:

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Kleinsorge teaches said router is re-configurable by altering said memory partition information, wherein said memory allocated to said plurality of processors is re-allocable (memory map can be reconfigured; 4/63-5/3).

As to claim 7,23:

Kleinsorge teaches said memory router comprises a first component and a second component, said first and said second components coupled by a communication link; said first component (memory address) operable to add a key to said memory access request, said key identifying said second processor; and said second component (memory map) operable to use said key to route said request to said address in said memory allocated to said second processor, wherein multiple processors using the same communication link and using overlapping addresses securely access said memory (the requested address is mapped using the memory map to allow access to the requested area 4/60-65; Abstract).

As to claim 8,21:

Kleinsorge teaches a said memory partition information is stored in a table containing a translation from processor address space to memory (memory map; 18/60-19/5).

As to claim 9:

Kleinsorge teaches said table further comprises information allocating to a first processor of said plurality read only access to a first memory partition and to a second processor read and write access to said first memory partition (setting access rights; 19/1-5).

As to claim 10:

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Kleinsorge teaches a more than one processor has access to a memory partition, wherein said memory is shared and said memory router has control over memory access (shared access rights; 18/60-19/5).

As to claim 11:

Kleinsorge teaches a said plurality of processors are coupled to said memory router via a single communication link (bus 122 ; Figure 1).

As to claim 12:

Kleinsorge teaches said plurality of processors are coupled to said memory router via a plurality of communication links (memory map is coupled to bus for memory mapping; Figure 1; 6/50-61; 18/60-19/5).

As to claim 13:

Kleinsorge teaches a first processor of said plurality runs a first operating system and said second processor of said plurality runs a second operating system and wherein said second processor is allowed to read the memory allocated to said first processor but is not allowed to write to said memory allocated to said first processor (privileged/restricted access; 18/60-19/5).

As to claim 16:

Kleinsorge teaches re-configuring said memory router with commands entered via an external port to said memory router, wherein software executing on said plurality of processors is unable to modify said memory router (reconfiguring by system manager; 4/55-67).

As to claim 20:

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Kleinsorge inherently teaches adding information to said memory request, said information specifying the processor of said plurality of processors which made said memory request, said plurality of processors sharing a communication link; and e) after receiving said memory request via said communication link, said memory router using said information to determine which processor made said memory request (request processor knows who the request is from; 9/30-37) .

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinsorge (US 6,247,109).

As to claim 4,18:


Kleinsorge does not specifically teach said type of access is selected from the group consisting of read only, write only, and read/write access. Kleinsorge does teach restricting access from non-privileged CPUs. One ordinary skills in the art would recognize that restricting access types such as read-only , write-only, and read/write only are examples of such access restriction. Thus it would have been obvious to one of ordinary skills to restrict access to certain

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access types; such as read-only , write-only, and read/write only to restrict access to certain restrict/privileged memory areas, as suggested by Kleinsorge.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866. The examiner can normally be reached on M-F from 8:00 a.m. to 3:00 p.m. EST.
7. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.
8. The fax phone number for Art Unit 2187 is 703-308-9051 or 703-308-9052.



Than Nguyen

Primary Patent Examiner

May 27, 2003



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

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Washington, D.C. 20231

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
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